Amendments to the Specification:

Please replace paragraph 0015 with the following amended paragraph:

Fig.4 is a circuit diagram of the adjusting module shown in ~~Fig.3~~ Fig.2.

Please replace paragraph 0025 with the following amended paragraph:

When the driving voltage supplied by the power supply module in a device is between the voltage level of V_H and the voltage level of $(V_s)_2$, the memory chip utilizing the voltage clamper 10 can function normally in the device. Similarly, the memory chip utilizing the voltage clamper 10 can function normally in the device when the driving voltage supplied by the power supply module is between the voltage level of $(V_s)_1$ and the voltage level of $(V_s)_2$, and between the voltage level of V_{bot} and the voltage level of $(V_s)_1$. However, there is a problem when the driving voltage supplied by the power supply module approaches $(V_s)_1$ or $(V_s)_2$. It is known that the predetermined voltage level originally set by the voltage detection units 20a, 20b will control the voltage clamper 10 to trigger the output voltage V_{out} to generate changes of the voltage levels, when the voltage levels of the input voltage V_{in} are $(V_s)_1$ and $(V_s)_2$. In other words, the output voltage V_{out} will hop between two voltage levels if vibration of the driving voltage supplied by the power supply module occurs in the neighborhood of the voltage level of $(V_s)_1$ or $(V_s)_2$. As a result, the memory chip generates unexpected errors. In order to resolve the problem, the voltage detection unit 20a further comprises an adjusting module 44 and the voltage detection unit 20b further comprises an adjusting module 46. The adjusting modules 44, 46 are used for adjusting the predetermined voltage levels detected by the voltage detection units 20a, 20b. Please refer to Fig.4.

Fig.4 is a circuit diagram of the adjusting module shown in ~~Fig.3~~ Fig.2. It is worth noting that only the adjusting module 44 is illustrated because the configuration and the operation of the adjusting module 44 and the adjusting module 46 are the same. The adjusting module 44 comprises a plurality of transistors 48. A drain of each of the transistors 48 is connected to a node A' of the voltage detection unit 20a, and a gate of each of the transistor 48 is selectively connected to a source of the transistor or an input terminal A of the voltage detection unit 20a. When the gate of the transistor 48 is connected to the input terminal A of the voltage detection unit 20a, the transistor 48 is regarded as being in parallel with the transistor 28b. Therefore, the transistor 48 can be utilized to adjust the predetermined voltage level at the input terminal A detected by the voltage detection unit 20a. Oppositely, the transistor 48 cannot be turned on and will not affect the operation of the voltage detection unit 20a when the gate of the transistor is connected to the source of the transistor. In this preferred embodiment, the gate of each of the transistor 48 is connected to the node A' or the source of the transistor is programmed by an upper level metal layer. That means the metal layer is utilized to program the adjusting module 44. For example, the initial setting of the adjustment module 44 is achieved by programming the upper level metal layer through a mask pattern design during the semiconductor processes for forming the voltage clamper 10, and the initial setting of the adjusting module 44 is that the gates of half of the transistors 48 are connected to the input terminal A and the gates of half of the transistors 48 are connected to the sources of the corresponding transistors 48. At this time, the characteristic of the input voltage V_{in} and the output voltage V_{out} of the voltage clamper 10 is shown in Fig.3. If it is known that the driving voltage supplied by the power supply module in a device approaches the voltage level of $(V_s)_1$, another

mask pattern design is utilized during the semiconductor processes for forming the voltage clamper 10. The numbers of the transistors 48 having the gates connected to the sources of the transistors 48 and the numbers of the transistors 48 having the gates connected to the input terminal A are thus adjusted to bias the voltage level of $(V_s)_1$. In addition, the adjust module 44 can lower the voltage level of $(V_s)_1$ or lift the voltage level of $(V_s)_1$. Therefore, the problem that the output voltage V_{out} probably changes greatly due to the input voltage V_{in} approaching the original voltage level of $(V_s)_1$ is avoided. Since the operation of the adjusting module 46 is the same as that of the adjusting module 44, the adjust module 46 can lower the voltage level of $(V_s)_2$ or lift the voltage level of $(V_s)_2$ in this preferred embodiment. As a result, the problem that the output voltage V_{out} probably changes greatly due to the input voltage approaching the original voltage level of $(V_s)_2$ is avoided. In summary, the devices having the voltage clamper 10 can operate more stably by utilizing the adjusting modules 44, 46.